In the Specification:

Please amend the specification as follows:

[0019] To achieve at least one of these objects, a multilevel reference generator has a plurality of standard resistive elements such as multilevel magnetic tunnel junctions set to differing parallel and anti-parallel magnetic orientations. Each resistive element is biased at a constant level to impart a resultant level from each resistive element. If the constant level is a constant voltage, the resultant levels of the plurality of resistive elements and the mirrored replications are currents. Alternately, the constant level is a constant current and the resultant levels of the plurality of resistive elements and the mirrored replications are voltages. ~~Further, each resistive element has a resistance different from the resistance of each of the plurality of restive elements.~~

[0038] Returning to Fig. 5, the source of the biasing transistor **225** is connected to establish the constant voltage level $\mathbf{V_A}$ **220**. The gate of the biasing transistor **225** is connected to a biasing voltage source $\mathbf{V_{BIAS}}$ **230**, thus establishing the constant voltage level $\mathbf{V_A}$ **220** as the voltage level of the biasing voltage source $\mathbf{V_{BIAS}}$ **230** plus the threshold voltage (Vt) of the biasing transistor **225**. The current $\mathbf{I_n}$ **235** is then determined by the formula:

$$I_n = \frac{V_A}{\left(R_{MTJ1}R_{MTJ2}\right)\Big/\left(R_{MTJ1}+R_{MTJ2}\right)}$$ ~~(delete prior formula and replace)~~

[0042] The reference current $\mathbf{I_{REF\_n}}$ **270** may be applied directly to the sense amplifier as a reference current. Alternately, as shown in Fig. [[8]] 7, the reference current $\mathbf{I_{REF\_n}}$ **270** of the reference current generator **275** may be applied within the multilevel reference generator of this invention to a reference resistor **280**. The voltage across the reference resistor **280** then becomes the reference voltage $\mathbf{V_{REF\_n}}$.

[0043] Fig. [[7]] 8 illustrates the whole reference generation sub-circuit **300** necessary to provide one of the reference levels of a multilevel reference generation circuit of this invention. The reference generation sub-circuit **300** as shown creates the first reference voltage $\mathbf{V_{REF\_1}}$ **380** that

is developed from the reference current $\mathbf{I_{REF\_1}}$ **370**. The reference generation sub-circuit 300 includes a first nonlinear resistive element **305**. The first nonlinear resistive element [[**310**]] is formed by combining two MTJ devices **307** and **309** connected in parallel. The two MTJ devices **307** and **309** have their magnetic fields set to be parallel. This makes the resistance level of the two MTJ devices **307** and **309** at their minimum values and any current through them at the maximum value when they are biased at a constant voltage level $\mathbf{V_A}$ **315**.

[0045] A first mirror source **330** is connected to provide the resultant current $\mathbf{I_1}$ **320** and a first mirrored replication current $\mathbf{I_1MIRROR}$ **335** of the resultant current $\mathbf{I_1}$ **320**. The first mirror source is formed by connecting the MOS transistors **332** and **334** such that their gates are connected together and to the drain of the biasing transistor **325** and the drain of the MOS transistor **332**. The first mirrored replication current $\mathbf{I_1MIRROR}$ **335** flows from the drain of the MOS transistor **334**.

[0046] The reference generation sub-circuit **300**, further, includes a second nonlinear resistive element **310**. The second nonlinear resistive element **310** is formed of two MTJ devices **312** and **314** connected in parallel. The two MTJ devices **312** and **314** have their magnetic fields set to be such that the MTJ device **312** is parallel and the MTJ device **314** is anti-parallel. This makes the resistance level of the MTJ device **312** at its ~~maximum~~ minimum value and the resistance level of the MTJ device **314** at its ~~minimum~~ maximum value and any current through them at an intermediate value when they are biased at a constant voltage level $\mathbf{V_A}$ **315**.

[0048] A second mirror source 355 is connected to provide the resultant current I_2 [[350]] 345 and a second mirrored replication current I_2MIRROR 360 of the second resultant current I_2 345. The second mirror source 355 is formed of the MOS transistors 357 and 359 having their gates connected together and to the drain of the biasing transistor 350 and the drain of the MOS transistor 357. The second mirrored replication current I_2MIRROR 360 flows from the drain of the MOS transistor 359.